REMARKS/ARGUMENTS

In response to the Office action identified above, please accept the following remarks.

1. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman et al. US patent NO. 6,605,838, in view of Nitayama et al. US patent No. 6,236,079.

Response:

According to claim 1, the present application discloses that an annular drain and an annular source are placed around the deep trench and circularly encompass the deep trench for forming an annular channel to raise sufficient current. In addition, the present application's vertical transistor and trench capacitor are isolated from other transistor by the STI.

MPEP 2142 reads in part:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both

be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Because Nitayama et al. discloses semiconductor memory devices of a planar transistor structure that is different from the vertical transistor of present application, the references cannot be combined in the manner relied upon by the office action because the prior arts do not teach the desirability of combination.

In connection with the first criteria of the *prima facie* case of obviousness, MPEP 2143.01 states that the prior art must teach the desirability of the claimed invention. The mere fact that references can be combined or modified does not render the result combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills,* 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

Applicant submits that the office action fails to show suggestion or motivation to combine the reference teachings insofar as the desirability of the combination is not taught in the prior arts. Namely, the office action simply states" It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the gate and drain contact to the structure taught by Nitayama in the structure of Mandenlman in order to make contact to other portion of the integrated circuit", and " to incorporate the STI structures taught by Nitayama in the structure of Mandenlman in order to provide better isolation".

Furthermore, the Examiner indicates that Nitayama et al. (US

6,236,079) teachs forming a contact structure 112 on a gate conductive layer 124.

However, the disclosure of Nitayama et al. is the combination of the dynamic semiconductor memory of a planar transistor and trench capacitor. Refer to Fig.4A and 4B, each gate electrode 136 of planar transistor including a polysilicon layer 136a and a silicide layer 136b is a portion of word line 136 (col. 4, lines 16 and 64). Therefore, **Nitayama et al. fails to teach that the first contact plug 112 is fabricated on the gate electrode 136** in any figure or in specification.

Moreover, the structure notified by number 124 is a "second trench fill" not the gate conductive layer stated in the office action. And the contact plug 112 is electrically connected between the trench capacitor and the transfer gate (col.4 lines 30-32), but the first contact plug of present invention is isolated from the trench capacitor.

Figs.4A and 4B are cross-sectional views of Fig.3, so Figs.4A and 4B are the same structure. As shown in Fig.4B, the STI 108 is adjacent to the drain 134, and isolates the drain 134 and other devices. Another transistor or drain is not shown in Fig.4B, so it cannot be known that the drain 134 is isolated from other drain-isolation of transistors. Nevertheless, as shown in Fig.4A, it is clear that the drain 134 is a community drain of two adjacent transistors (col.4, lines 59-60), so Nitayama et al. never teach that an STI isolates a drain from other drains of adjacent transistors.

To sum up, the Nitayama et al. fails to teach the present application's

claim 1 limitation of forming a contact structure on a gate conductive layer, and using an STI positioned around the deep trench and isolating a drain of vertical transistor and a drain of other transistors.

Even when taken in combination, Nitayama et al. and Mandelman et al. fail to teach or suggest to form the gate conductive layer electrically connected to a first contact plug, and using an STI positioned around the deep trench and isolating a drain of vertical transistor and a drain of other transistors.

In connection with the third criteria, MPEP 2143.03 goes on the state:

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Applicants respectfully assert that none of the three criteria are met to sustain a 35 U.S.C. 103(a) rejection against claim 1 when combining Nitayama with Mandelman's application. Therefore, reconsideration of claim 1 is politely requested.

Referring to claims 4 and 5 of this application, the Examiner points out that Mandelman et al. teach a buried strap (86) but the buried strap is a drain/source diffusion region (col. 5, lines 10-20). The buried strap of present application is located on the inner surface of the sidewall of the deep trench, so the buried strap of the present application is different from

the drain/source diffusion region of Mandelman et al.. Reconsideration of claim 4 and amended claim 5 is hereby respectfully requested.

Since claims 2-5, 7-8 and 10-11 are dependent upon the amended claim 1, they should be allowed if the amended claim 1 is allowed. Reconsideration of claims 2-5, 7-8 and 10-11 are hereby respectfully requested.

Referring to claim 6 of this application, Nitayama et al. never teach forming a contact plug on a gate electrode. As shown in Fig. 4A, the gate electrode 136 including a polysilicon layer 136a and silicide layer 136b (col. 4, lines 64-66), and conductive layer are deposited on the gate electrode 136 and make the gate electrode 136 electrically connected to another contact plug. Reconsideration of claim 6 is hereby respectfully requested.

Referring to claim 9 of this application, the passivation layer directly covers the surface of the transistor 166 and the substrate 110, but Fig.4B of Nitayama et al. shows that the second isolation layer 152 is deposited on the word line 102 and the first isolation layer 148, and does not contact the substrate and transistor. Therefore, the second isolation layer 152 of Nitayama et al. is different from this application. In addition, the first isolation layer 148 of Nitayama et al. is a planar transistor, but does not contact the surface of the substrate 114, so the position of the first isolation layer 148 is different from the position of the conductive layer of the present application. Reconsideration of claim 9 is hereby respectfully requested.

Referring to claim 12 of this application, an annular spacer 150 of the present application is deposited on a surface of a sidewall of the upper deep trench 120 and circularly encompassing the deep trench 120. The Examiner compares the present application's sidewall with the sidewall 140 of Nitayama et al.. However, the sidewall 140 of Nitayama et al. is a uniform silicon nitride barrier layer 140 (col. 5, lines 1-4) but not a general sidewall. Nitayama et al. fails to teach utilizing the method of sidewall replaced deposit process to manufacture the silicon nitride barrier layer 140. In addition, as shown in Fig.4B, the silicon nitride barrier layer 140 of Natayama et al. is not circularly encompassing the deep trench by sidewall structure. Reconsideration of claim 12 is hereby respectfully requested.

Referring to claim 13 of this application, similar to the above-mentioned discussion, the silicon nitride barrier layer 140 of Natayama et al. is not a sidewall, so Natayama et al. never teach a second contact plug is directly deposited on the drain and the sidewall. As shown in Figs.3, 4A, and 4B, the contact plug 106 is a symmetrical structure deposited between two transistors, so Natayama et al. is different from the present application. Reconsideration of claim 13 is hereby requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

Winston Hsu Date: April 22, 2005

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan).